6   a first bus bridge coupled to the first bus and to the second bus, the first

7   bus bridge providing a path for transferring data between the first memory and

8   the second processor;

9   a second memory coupled to the first bus;

10   a second bus bridge coupled to the second bus and a third bus, the third

11   bus providing a data pathway within the first processor, the second bus bridge

12   providing a path for transferring data between the second memory and the third

13   bus of the first processor; and

14   a direct memory access (DMA) controller coupled to the second bus, the

15   DMA controller configured to manage a transfer of data between the second

16   memory and the second bus bridge;

17   wherein the first processor is configured to operate at a first frequency, the

18   second processor is configured to operate at a second frequency, and the first

19   frequency is greater than the second frequency, and wherein the first bus and the

20   second bus are dissimilar.

1   18. (New) The electronic product of Claim 17, wherein the first processor and the

2   second processor are both disposed together on a single integrated circuit.

1   19. (New) The electronic product of Claim 18, wherein the first processor is a

2   digital signal processor, and the second processor is a microcontroller.

1   20. (New) The electronic product of Claim 18, wherein a first portion of the first
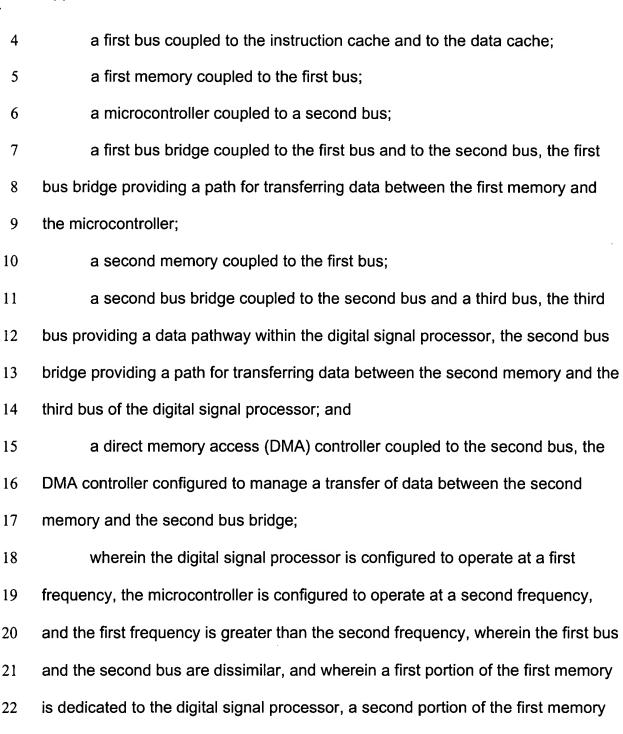
14

2 memory is dedicated to the first processor, a second portion of the first memory

3 is dedicated to the second processor, and a third portion of the first memory is

4 shared by the first and the second processors.

1 ~~52~~4. (New) The electronic product of Claim ~~20~~ 4, wherein the first bus has a first

2 width, the second bus has a second width, and the third bus has a third width;

3 the first width is greater than the second width, and the second width is greater

4 than the third width.

1 ~~22~~6. (New) The electronic product of Claim ~~21~~ 5, wherein the DMA controller and

2 the second bus are both disposed on the single integrated circuit.

1 ~~23~~7. (New) The electronic product of Claim ~~22~~ 6, wherein the first bus has a width of

2 128 bits, the second bus has a width of 32 bits, and the third bus has a width of

3 16 bits.

1 ~~24~~8. (New) The electronic product of Claim ~~22~~ 6, further comprising a Read Only

2 Memory (ROM) disposed on the single integrated circuit and coupled to the

3 second bus.

1 ~~25~~9. (New) A mobile radiotelephony controller, comprising:

2 a digital signal processor coupled to an instruction cache and to a data

3 cache;

3

4   a first bus coupled to the instruction cache and to the data cache;

5   a first memory coupled to the first bus;

6   a microcontroller coupled to a second bus;

7   a first bus bridge coupled to the first bus and to the second bus, the first

8   bus bridge providing a path for transferring data between the first memory and

9   the microcontroller;

10   a second memory coupled to the first bus;

11   a second bus bridge coupled to the second bus and a third bus, the third

12   bus providing a data pathway within the digital signal processor, the second bus

13   bridge providing a path for transferring data between the second memory and the

14   third bus of the digital signal processor; and

15   a direct memory access (DMA) controller coupled to the second bus, the

16   DMA controller configured to manage a transfer of data between the second

17   memory and the second bus bridge;

18   wherein the digital signal processor is configured to operate at a first

19   frequency, the microcontroller is configured to operate at a second frequency,

20   and the first frequency is greater than the second frequency, wherein the first bus

21   and the second bus are dissimilar, and wherein a first portion of the first memory

22   is dedicated to the digital signal processor, a second portion of the first memory

23   is dedicated to the microcontroller, and a third portion of the first memory is

24   shared by the digital signal processor and the microcontroller.

1   26. (New) The mobile radiotelephony controller of Claim 25, further comprising a